AMENDMENTS TO THE CLAIMS

A listing of the claims of the present application, which are amended herein with markings to show changes made, is provided below:

Claims 1-20 (Cancelled).

Claim 21 (Currently Amended) A semiconductor structure comprising:

at least one first semiconductor area with a first trench isolation region and a first sidewall between said first semiconductor area and said first trench isolation region, wherein said first trench isolation region surrounds said first semiconductor area and comprises silicon oxide and ~~at least a portion of~~ said first sidewall is void of any nitride liner; and

at least one second semiconductor area with a second trench isolation region and a second sidewall between said second semiconductor area and said second trench isolation region, wherein said second trench isolation region surrounds said second semiconductor area and comprises silicon oxide and a nitride liner is present on ~~at least a portion of~~ said second sidewall.

Claim 22 (Previously Presented) The semiconductor structure of Claim 21, wherein said first semiconductor area is under a first compression stress and said second semiconductor area is under a second compression stress and the level of first compression stress is higher than the level of second compression stress.

Claim 23 (Currently Amended) The semiconductor structure of Claim 21, wherein ~~the entirety of said first sidewall surrounding said first semiconductor area is void of any nitride liner and~~ said

nitride liner is present on the entirety of said second sidewall surrounding said second semiconductor layer.

Claim 24 (Previously Presented) The semiconductor structure of Claim 21, wherein substantially no bird's beak structure is present between said first semiconductor area and said first trench isolation region.

Claim 25 (Previously Presented) The semiconductor structure of Claim 21, wherein at least one bird's beak structure is present between said second semiconductor area and said second trench isolation region.

Claim 26 (Previously Presented) The semiconductor structure of Claim 21, wherein substantially no bird's beak structure is present between said first semiconductor area and said first trench isolation region and at least one bird's beak structure is present between said second semiconductor area and said second trench isolation region.

Claim 27 (Previously Presented) The semiconductor structure of Clam 21, wherein said first semiconductor area includes at least one PFET and said second semiconductor area includes at least one NFET.

Claim 28 (Previously Presented) The semiconductor structure of Claim 21, further comprising an oxide layer on the first sidewall and an oxide layer on the second sidewall.

Claim 29 (Previously Presented) The semiconductor structure of Claim 21, wherein said nitride liner is a nitride surface layer that has a thickness of about 0.1 nm to about 2.0 nm.

Claim 30 (Previously Presented) The semiconductor structure of Claim 21, wherein a nitride liner is present on at least a portion of a bottom of said first trench isolation region.

Claim 31 (Previously Presented) The semiconductor structure of Claim 21, wherein at least a portion of a bottom of said second trench isolation region is void of any nitride liner.

Claim 32 (Currently Amended) A semiconductor structure comprising:

a trench isolation region;

at least one first semiconductor area with a first sidewall that adjoins said trench isolation region; and

at least one second semiconductor area with a second sidewall that adjoins said trench isolation region, wherein ~~at least a portion of~~ said first sidewall is void of any nitride liner and a nitride liner is present on ~~at least a portion of~~ said second sidewall.

Claim 33 (Previously Presented) The semiconductor structure of Claim 32, wherein said first semiconductor area is under a first compression stress and said second semiconductor area is under a second compression stress and the level of first compression stress is higher than the level of second compression stress.

Claim 34 (Previously Presented) The semiconductor structure of Claim 32, wherein the entirety of said first sidewall is void of any nitride liner and said nitride liner is present on the entirety of said second sidewall.

Claim 35 (Previously Presented) The semiconductor structure of Claim 32, wherein substantially no bird's beak structure is present between said first semiconductor area and said trench isolation region.

Claim 36 (Previously Presented) The semiconductor structure of Claim 32, wherein at least one bird's beak structure is present between said second semiconductor area and said trench isolation region.

Claim 37 (Previously Presented) The semiconductor structure of Clam 32, wherein said first semiconductor area includes at least one PFET and said second semiconductor area includes at least one NFET.

Claim 38 (Previously Presented) The semiconductor structure of Claim 32, further comprising an oxide layer on the first sidewall and an oxide layer on the second sidewall.

Claim 39 (Previously Presented) The semiconductor structure of Claim 32, wherein said nitride liner is a nitrided surface layer that has a thickness of about 0.1 nm to about 2.0 nm.

Claim 40 (Previously Presented) The semiconductor structure of Claim 32, wherein said first sidewall does not adjoin said second sidewall.